



Linko Semiconductor Co. Ltd.

LKS513 Datasheet

@ 2019, All rights reserved by Linko
Confidential documents, non-proliferation without
permission

1 Summary

1.1 Description

The LKS513 is a three-phase 40V, high speed half-bridge pre-driver for power P/N MOSFET. It has two inputs for high side and low side, and two outputs per channel with internal dead time to avoid cross-conduction.

The input logic level is compatible with 3.3V/5V/15V signal. Output 10V gate voltage for both PMOS and NMOS.

It also built in a 5V/30mA LDO for MCU or other device power supply, and have thermal shut down protection for safety.

1.2 Features

- Three-phase outputs for P/N MOS half-bridge
- Operation supply range from 8V to 28V
- Independent inputs for high side and low side
- Output 10V ($V_{CC} > 10V$) V_{GS} for both PMOS and NMOS
- 3.3V, 5V and 15V input logic compatible
- Built-in 5V / 30mA LDO
- Built-in dead time
- Built-in TSD
- Available in ESOP16 package

1.3 Typical Application

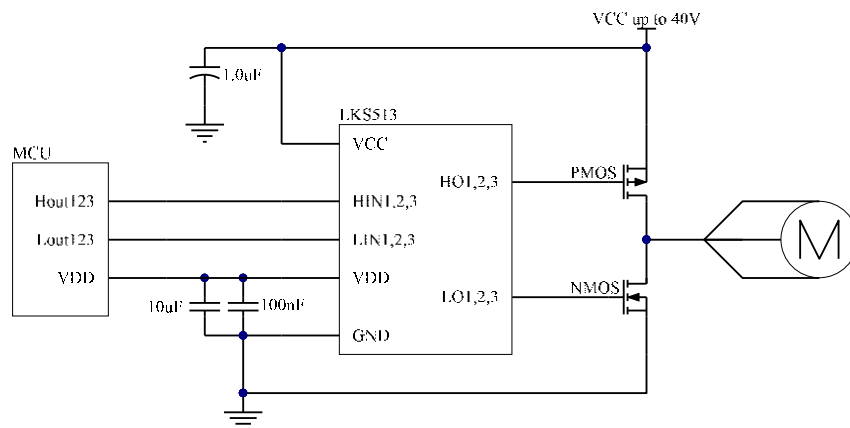


Figure 1-1 Typical Application Circuit

1.4 Internal Block Diagram

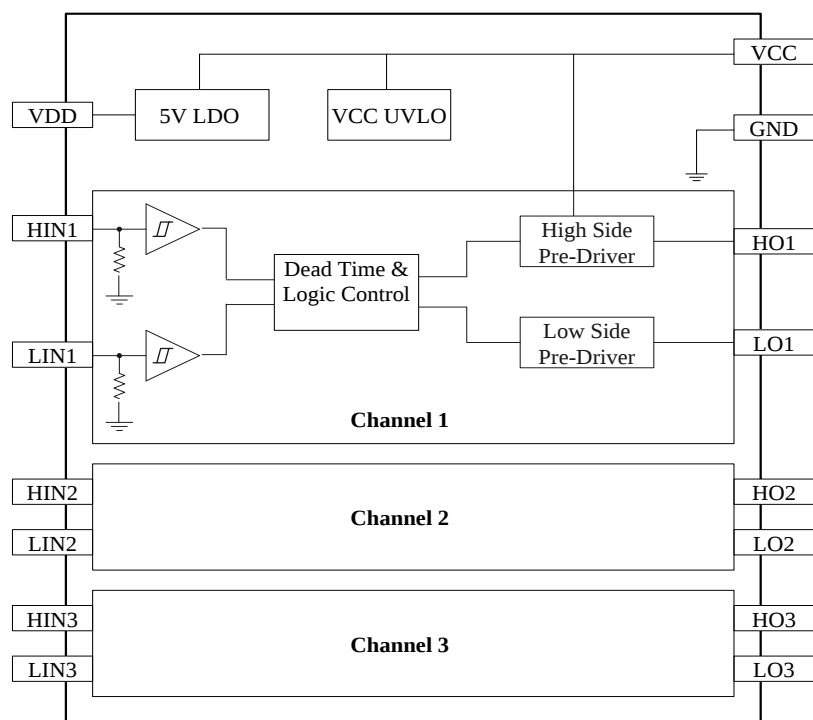


Figure 1-2 Internal Block Diagram

1.5 Waveforms

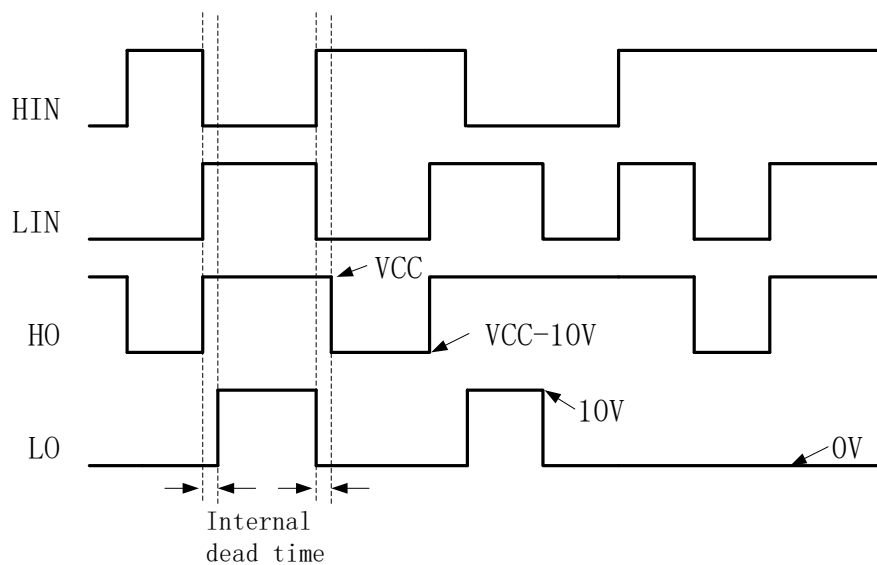


Figure 1-3 Input/output Timing Diagram

2 Pin Configuration and Ordering Information

2.1 Pin Diagram

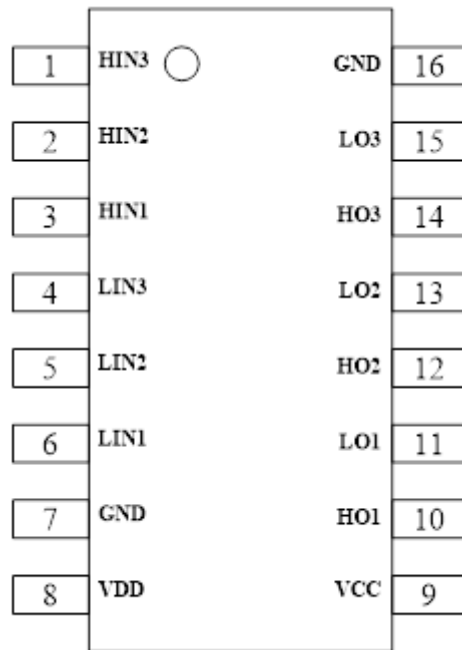


Figure 0-1 Pin Configuration

2.2 Pin Definition

Table 0-1 Pin definition

Pin No.	Name	Description
1	HIN3	Logic input for high side channel 3
2	HIN2	Logic input for high side channel 2
3	HIN1	Logic input for high side channel 1
4	LIN3	Logic input for low side channel 3
5	LIN2	Logic input for low side channel 2
6	LIN1	Logic input for low side channel 1
7	GND	Ground, short to pin 16
8	VDD	5V LDO reference output
9	VCC	Power supply voltage
10	HO1	High side driver output channel 1
11	LO1	Low side driver output channel 1

12	HO2	High side driver output channel 2
13	LO2	Low side driver output channel 2
14	HO3	High side driver output channel 3
15	LO3	Low side driver output channel 3
16	GND	Ground, short to pin 7

2.3 Ordering Information

Part Number	Package	Operation Temperature	Package Method	Marking
LKS513	ESOP16	-40 °C to 105 °C	Tape TBD Piece/Roll	LKS513 XXXXXXYX XXWWE



3 Physical Dimensions

ESOP16 Package:

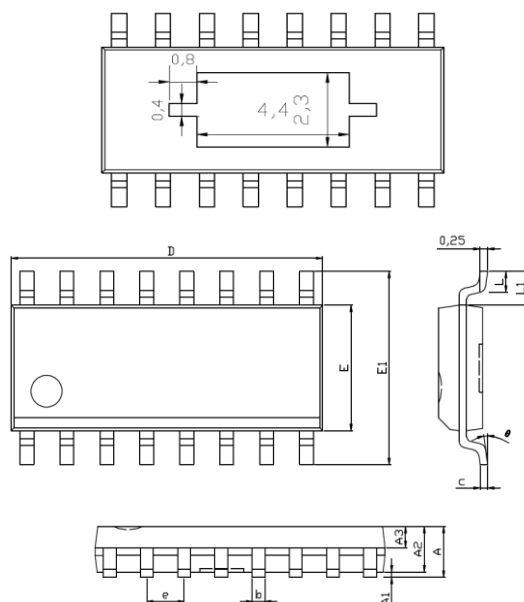


Figure 0-1 Packaging Graphic

Table 0-1 LKS513 Package size

Symbol	Dimensions In Millimeters	
	Min.	Max.
A		1.57
A1	0.00	0.07
A2	1.40	1.50
A3	0.61	0.71
b	0.39	0.45
c	0.51	0.26
D	9.70	10.10
E	3.70	4.10
E1	5.80	6.20
e	1.24	1.30
L	0.60	0.80
L1	0.99	1.10
θ	0°	8°

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Table 4-1 Absolute Maximum Ratings

Symbol	Parameters	Min.	Max.	Unit
V_{CC}	Power supply voltage	-0.3	40	V
V_{DD}	LDO output voltage	-0.3	5.5	V
I_{VDD}	LDO output current	-0.3	35	mA
$V_{HIN} V_{LIN}$	Input voltage	-0.3	20	V
V_{HO}	High side output voltage	-0.3	V_{CC}	V
V_{LO}	Low side output voltage	-0.3	15	V
P_{DMAX}	Package power dissipation	--	0.5	W
θ_{JA}	Thermal resistance, junction to ambient	--	105	°C/W
T_J	Junction temperature	-40	150	°C
T_{STG}	Storage temperature	-55	150	°C
	ESD	2		KV

4.2 Recommended Operation Conditions

Table 4-2 Recommended Operation Conditions

Symbol	Parameters	Min.	Max.	Unit
V_{CC}	Power supply voltage	8	28	V
$V_{IN(ON)}$	Input ON Threshold Voltage	2.9	V_{CC}	V
$V_{IN(OFF)}$	Input OFF Threshold Voltage	0	0.4	V
T_{DEAD}	MCU input dead time	0.5	--	us
F_{PWM}	PWM Switching Frequency	--	50	kHz

4.3 Dynamic Electrical Characteristics

Unless otherwise specified, $V_{CC} = 24V$, $C_L = 1000\text{ pF}$, $T_A = 25^\circ\text{C}$.

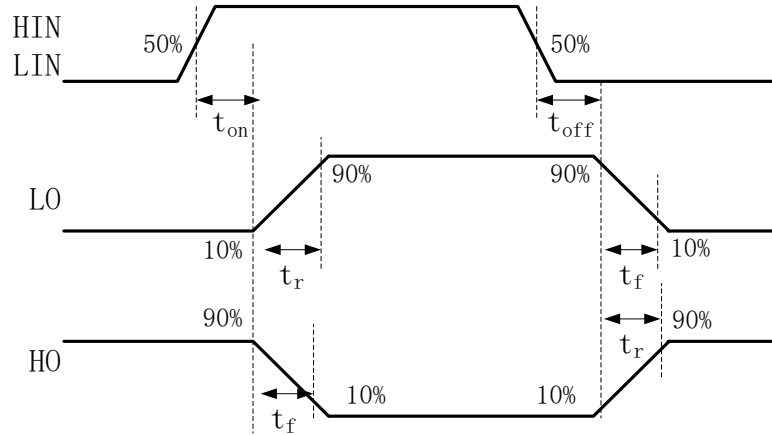


Figure4-1 Switching Timing Waveforms

Table4-3 Dynamic Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
T_{ON}	Turn-on propagation delay		-	80	-	ns
T_{OFF}	Turn-off propagation delay		-	30	-	
TH_R	HO rise time		-	60	-	
TH_F	HO fall time		-	300	-	
TL_R	LO rise time		-	300	-	
TH_F	LO fall time		-	60	-	
DT	Dead time		-	100	-	

4.4 Static Electrical Characteristics

Table 4-4 Static Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics						
V_{CC_ON}	V_{CC} under voltage rising threshold		5.8	6.5	7.4	V
V_{CC_UVLO}	V_{CC} under voltage falling threshold		5.4	6.0	6.8	V
V_{CC_HYS}	V_{CC} under voltage hysteresis voltage		0.3	0.5	0.8	V

I_{QCC}	Quiescent V_{CC} supply current	$HIN=LIN=0V$	0.3	0.5	1.0	mA
V_{DD}	VDD output voltage		4.7	5	5.3	V
V_{IH}	Logic “1” input voltage		2.2	-	-	V
V_{IL}	Logic “0” input voltage		-	-	0.6	V
$I_{ISOURCE}$	Logic “1” input bias current	$HIN, LIN=5V$	-	36	100	uA
I_{ISINK}	Logic “0” input bias current	$HIN, LIN=0V$	-	0	1	uA
V_{HO}	HO output voltage	$HIN=5V$	$VCC-11.5$	$VCC-10$	$VCC-8.5$	V
		$VCC<10V$	-	VCC	-	
V_{LO}	LO output voltage	$LIN=5V$	8.5	10	11.5	V
		$VCC<10V$	-	0	-	
I_{HO+}	HO sink current	$HO=VCC$	-	50	-	mA
I_{HO-}	HO source current	$HO=VCC-8V$	-	300	-	mA
I_{LO+}	LO source current	$LO=0V$	-	50	-	mA
I_{LO-}	LO sink current	$LO=8V$	-	300	-	mA
T_{SD}	TSD Temperature		-	150	-	°C
$T_{RECOVER}$	TSD release temperature		-	135	-	°C

5 Version History

Table 5-1 Document Version History

Time	Version number	Explain
2025.07.30	1.4	1.3 PMOS tube reverse
2023.05.23	1.3	Fix Typo
2020.04.24	1.2	Minor Revision
2020.01.05	1.1	Minor Revision
2019.12.30	1.0	Revisions for releases

